## AMENDMENTS TO THE SPECIFICATION

Please replace paragraph number **[0001]** with the following rewritten paragraph:

**[0001]** This application is a divisional application of U.S. patent application Ser. No. 09/945,042, now U.S. Pat. No. 6,686,654, filed August 31, 2001 entitled "MULTI-CHIP ~~ELECTRONIC PACKAGE~~ STACK AND COOLING SYSTEM." This application is also related to co-pending U.S. patent application Ser. No. 09/945,024, now U.S. Pat. No. 6,747,347, filed Aug. 30, 2001 entitled "MULTI-CHIP ELECTRONIC PACKAGE AND COOLING SYSTEM" the entirety of which is incorporated by reference.

Please replace paragraph number **[0023]** with the following rewritten paragraph:

**[0023]** References will now be made to the drawings wherein like numerals refer to like parts throughout. Figure 1 is a partial schematic illustration of one embodiment of an integrated circuit chip 100 that can be incorporated into a multiple chip stack structure of the preferred embodiment. As shown in Figure 1, the chip 100 comprises a substrate 102, such as a silicon substrate, that carries a variety of integrated circuitry and devices, such as capacitors, resistors, transistors, memory cells, and logic gates, that are formed using conventional semiconductor manufacturing processes. As also shown in Figure 1, the chip 100 further comprises a support frame 104, a plurality of air bridge structures 106, and a temporary support material 107 that are each formed on an upper surface 108 of the substrate 102 using methods known in the art or, more preferably, in accordance with methods described in Applicant's co-pending U.S. Patent Application No. 09/382,929, entitled "PACKAGING OF ELECTRONIC CHIPS WITH AIR-BRIDGE STRUCTURES", Attorney Docket No. 303.603US1, which is incorporated by reference herein in its entirety.

Please replace paragraph number **[0028]** with the following rewritten paragraph:

**[0028]** In one embodiment, the support frame 104 is fabricated by depositing a layer of metal on the upper surface 108 of the substrate 102 using chemical vapor deposition (CVD), plasma enhanced CVD (PECVD), physical vapor deposition (PVD) techniques, sputtering, and/or electroforming. The metal layer is subsequently patterned

and etched to define the configuration of the frame 104. In another embodiment, the support frame 104 and interconnection wiring for each wiring level are formed in the same process set using methods disclosed in Applicant's co-pending U.S. patent application no. 09/640,149, now U.S. Pat. No. 6,709,968, entitled "MICROELECTRONIC DEVICE WITH PACKAG~~ING~~E WITH CONDUCT~~OR~~IVE ELEMENTS AND ASSOCIATED METHOD OF MANUFACTURE", which is incorporated by reference herein its entirety. The support frame 104 can be made of a conductive material such as copper. Alternatively, the support frame 104 may comprise copper and an organic and/or inorganic insulating insert material. The insulating insert material is preferably incorporated in the reinforcement ribs 112 adjacent to where air bridge conductors are likely to extend through the ribs. In other embodiments, the support frame 104 may comprise an insulator made of organic and/or inorganic materials.

Please replace paragraph number **[0033]** with the following rewritten paragraph:

**[0033]** Figure 2 provides a partial schematic cross-sectional view of a chip stack 132 incorporating the chip 100 described and shown in Figure 1. The chip stack 132 comprises a plurality of chips 100 that are stacked together in a manner such that the upper surface 124 of the support frame 104 of one chip is positioned adjacent to a lower surface 134 of the substrate 102 of another chip. The chips 100 may be bonded to each other using C4 contacts and/or adhesives as described in the Applicant's co-pending U.S. Patent Application No. 09/932,859 entitled "A THREE DIMENSIONAL MULTI-CHIP STRUCTURE AND METHOD OF MAKING THE SAME", now U.S. Patent No. 6,433,413 issued August 13, 2002, which is incorporated by reference herein its entirety.

Please replace paragraph number **[0040]** with the following rewritten paragraph:

**[0040]** Furthermore, the exterior chips 214a-h can be mounted and interconnected to the chip stacks 202, 204 using C4 connections, modified C4 connections, and/or other methods disclosed in Applicant's co-pending U.S. Patent Applications, entitled "A THREE DIMENSIONAL MULTI-CHIP STRUCTURE AND METHOD OF MAKING THE SAME", U.S. Patent No. 6,433,413 issued August 13, 2002 and "ANGLED ~~INTERCONNECT~~ EDGE CONNECTIONS FOR MULTICHIP

STRUCTURES ", U.S. Patent Application No. 09/944,957 filed August 30, 2001, now U.S. Pat. No. 6,635,960, which are hereby incorporated by reference. As described above, in one embodiment, the distance between rows of conductive interconnects on adjacent chips in the chip stacks are precisely fixed by the upper portions of the support frame on each chip so that the interconnects may be aligned with electrical contacts such as, C4 connections, formed on the exterior chips.